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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,327	07/03/2003	Daniel M. Kinzer	IR-2143 (2-3569)	4291

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,327	KINZER ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the amendment on 12 October 2004. Claims 1-10 are pending; claims 11-17 have been cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi et al. (6,611,021) in view of Gardener et al. (6,204,153).

Onishi et al. disclose a process for the manufacture of a substrate for a superjunction device where a first epitaxial semiconductor layer (2a) of a given thickness and of a given impurity concentration of a first conductivity type is formed atop a support body (1); forming a plurality of laterally spaced implants (7) of a second conductivity type on the surface of the first epitaxial layer (2a) at vertically interior locations (Fig. 5c); forming a second epitaxial layer (2b) of a given thickness and of a given concentration and of the first conductivity type atop the first layer (2a) (col. 12, lines 33-63); heating the substrate (1) and the implants (7) to cause the implants (7) to diffuse downwardly into the first layer (2a) and upwardly into the second layer (2b), thereby forming spaced pedestals (58b) of the second conductivity type within the first and second layers (2a, 2b) (col. 8, lines 11-61); the total charge of each of the pedestals (58b) being approximately equal to the total charge in the volume of the first and second

layers (2a, 2b) which surrounds the pedestals (58b) (col. 13, lines 38-65); and thereafter forming MOSgated cell elements atop (16) each of the pedestals (58b). Onishi et al. further disclose the first and second layers (2a, 2b) having the same thickness and impurity concentration and the support layer (1) having the same conductivity type as the first and second layers (2a, 2b), wherein the first and layers together form a single epitaxial layer (col. 9, lines 15-36). Onishi et al. also disclose forming a drain electrode (18) on the bottom of the support layer (1), and separating the support layer (1) and the MOSgated cell elements (16) into separate unitary elements (col. 7, lines 20-51).

Onishi et al. do not disclose the first and second layers being silicon, the support body as a silicon wafer and the pedestals spaced from the support body.

Gardner et al. disclose a process for the manufacture of a substrate for a semiconductor device where a first epitaxial semiconductor layer (12) of a given thickness and of a given impurity concentration of a first conductivity type is formed atop a support body (10); forming a second epitaxial layer (14) of a given thickness and of a given concentration and of the first conductivity type atop the first layer (12) (col. 6, lines 25-64); forming an implant (26) of a second conductivity type on the surface of the first layer (12), where the implant (26) is spaced from the support body (10) (col. 8, lines 7-62); and thereafter forming a MOSgated cell element (30) atop of the implant (26) (col. 9, lines 6-53). Gardner et al. further disclose the first and second layers (12, 14) being silicon and the support body (10) as a silicon wafer (col. 6, lines 25-64).

Since Onishi et al. and Gardner et al. are both from the same field of endeavor, a process for the manufacture of a substrate for a semiconductor device, the purpose

disclosed by Gardner et al. would have been recognized in the pertinent art of Onishi et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Onishi et al. by the first and second layers being silicon, the support body as a silicon wafer and spacing the implant from the support body as taught by Gardner et al. to reduce punchthrough (col. 3, lines 17-34).

Response to Arguments

Applicant's arguments filed 12 October 2004 have been fully considered but they are not persuasive. As stated above, Onishi et al. in view of Gardner et al. disclose the process for the manufacture of a substrate for a superjunction device as described in claims 1 and 7.

In response to the applicant's arguments, the applicant argues that Onishi et al. teach the pedestals reaching the substrate. However, Gardner et al. disclose ion of a second conductivity type diffusing into first and second epitaxial layer not reaching the substrate (Fig. 4; col. 8, lines 7-25). Applicant further argues prior art does not teach multiple epitaxial layers. However, both Onishi et al. and Gardner et al. disclose multiple epitaxial layers. Applicant also argues prior art does not teach the pedestals near a central region of the single epitaxial layer. However, applicant does not claim the pedestals near a central region. Even if applicant claimed the pedestals near a central region, Gardner et al. teaches form the implant in a central region of the epitaxial layer (Fig, 4-7).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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